IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 18, with the following rewritten paragraph:

Referring to FIG. 1, a conventional semiconductor device may comprise device isolation layer 12 disposed in a predetermined region of a semiconductor substrate. The device isolation layer 12 may comprise an outline that defines first and second active regions in respective N-type and P-type regions 10a, 10b of the substrate. A PMOS transistor may be formed on the first active region of N-type region 10a between sidewalls ~~13A~~ 13a of isolation layer 12. Likewise, an NMOS transistor may be formed on the second active region of the P-type region 10b between sidewalls ~~13B~~ 13b of isolation layer 12.

Please replace the paragraph beginning on page 1, line 31, with the following rewritten paragraph:

As shown in FIG. 1, such conventional semiconductor device may further comprise well bias regions 18a and ~~18B~~ 18b for enabling connection of respective N-well and P-well regions to receive respective well or substrate body biasings. Well bias regions 18a and 18b may be formed separate from their respective transistors but within the active regions of the transistors.

Please replace the paragraph beginning on page 2, line 8, with the following rewritten paragraph:

For this example, further referencing the conventional device of FIG. 2, device isolation layer 22 may be formed in a predetermined region of the semiconductor substrate 20 and with sidewalls 23 forming an outline to define a plurality of active regions. Transistors may be formed on the respective active regions. Each well bias region 28 which may be associated with a group of the plurality of the transistors may be coupled to a common well bias region 28. Unfortunately, however, the single common well bias region 28 of such conventional ~~device~~ device, as shown in ~~FIG. 2~~ FIG. 2, may adversely affect an integrity of transistors 25 that may be more distant from well bias region 28. Such distant transistors may be more vulnerable to latch-up phenomenon or abnormal noise.

Please replace the paragraph beginning on page 5, line 17, with the following rewritten paragraph:

The first gate pattern g1 may comprise, in this embodiment, first gate electrode 108a that crosses the first active region 104a and gate insulation layer 106a disposed between the first gate electrode 108a and a surface of first active region 104a. Additionally, a first sidewall spacer 112a that may be formed of insulating ~~material~~ material, may cover a sidewall of first gate electrode 108a. This "sidewall spacer" may be referenced alternatively as simply a "spacer".

Please replace the paragraph beginning on page 6, line 13, with the following rewritten paragraph:

In this embodiment of the invention, the device isolation layer 102 adjacent to one of the P-type source/drain regions 116a of each PMOS transistor may be formed with a first recess 120a. The recess may expose a surface of the N-type region ~~100b~~ 100a adjacent to the selected one of the P-type source/drain region 116a neighboring the recess. The salicide layer 124a over the selected P-type source/drain region 116a may further comprise a portion that extends within first recess 120a to cover the exposed surface of N-type region ~~110b~~ 100a within the recess.

Please replace the paragraph beginning on page 6, line 20, with the following rewritten paragraph:

Likewise, a region of device isolation layer 102 adjacent to one of the N-type source/drain regions 116b of the NMOS transistor may also be formed with a recess (a second recess 120b). A surface of P-type region 100b adjacent to the one N-type source/drain region 116b neighboring the recess may face inwardly and be exposed by the second recess 120b. The salicide layer 124b on the neighboring N-type source/drain region 116b may further comprise a portion that extends beyond the source/drain region and into the second recess to cover the surface of P-type region ~~110b~~ 100b that was exposed and faces inwardly to the recess.

Please replace the paragraph beginning on page 7, line 5, with the following rewritten paragraph:

Referencing FIGS. 4 through 8, a method of fabricating a semiconductor device according to an embodiment of the present invention may include forming device isolation

layer 102 in a predetermined region of a semiconductor substrate as shown in Fig 4. An outline of the isolation layer may define first and second active regions 104a and 104b in N-type and P-type regions 100a and 100b, respectively. The N-type region 100a may comprise a conventional N-well that may be formed by doping N-type impurity ions into a P-type silicon substrate. The P-type region 100b may comprise a typical P-well that may be formed by doping P-type impurity ions into the silicon substrate or into N-well ~~110a~~ 100a.

Please replace the paragraph beginning on page 7, line 13, with the following rewritten paragraph:

Referring to FIG. 5, first and second gate insulation layers 106a and 106b may be formed on first and second active regions 104a and 104b, respectively. The first and second gate insulation layers 106a and 106b may comprise same materials of same or, alternatively, different thicknesses. A gate conductive layer [[108 ]]may be formed over the substrate and over the first and second gate insulation layers 106a and 106b. The gate conductive layer may comprise a doped polysilicon and may also comprise a metal silicide layer.

Please replace the paragraph beginning on page 8, line 10, with the following rewritten paragraph:

After forming ~~the~~ first sidewall spacers ~~112~~ 112a, the first gate pattern g1 may serve as an ion implantation mask while P-type impurity ions may be implanted into the first active region 104a. Such implant may form heavily diffused layer 114a of P-type impurities into regions of the first active region 104a at opposite sides of the first gate pattern g1. Likewise, N-type impurity ions may be implanted into second active region 104b while using the second gate pattern g2 as an ion implantation mask. Such implant may form N-type heavily diffused region 114b into regions of the second active region 104b on opposite sides of the second gate pattern g2. The heavily diffused layer 114a and lightly diffused layer 110a of P-type impurities may be described collectively as a source/drain ~~regions~~ region 116a of the PMOS transistor. The N-type heavily diffused layer 114b and the N-type lightly diffused layer 110b, similarly, constitute source/drain regions 116b of the NMOS transistor.

Please replace the paragraph beginning on page 8, line 21, with the following rewritten paragraph:

Next, further referencing FIG. 6, a photoresist pattern 118 may be formed on an entire surface of the resultant structure where the P-type and N-type source/drain regions 116a and

116b have been formed. Photoresist may be patterned to expose a predetermined region of the device isolation layer 102 adjacent to one of the P-type source/drain regions 116a as well as to expose a predetermined region of the device isolation layer 102 adjacent to one of the N-type source/drain regions 116b. While using the photoresist pattern 118 as an etch mask, the exposed regions of the device isolation layer 102 may be partially etched to form first and second recess 120a and 120b as shown in FIG. 7. The first and second recesses 120a and 120b, may be formed adjacent to one of the P-type source/drain regions 116a and one of the N-type source/drain regions 116b, respectively. The N-type region 100a of the substrate under the P-type source/drain region 116a may comprise a surface region 117a that may be exposed within first recess 120a. Similarly, P-type region 100b of the well under the N-type source/drain region 116b may comprise a surface 117b that may be exposed [[to ]]within the second recess 120b.

Please replace the paragraph beginning on page 9, line 30, with the following rewritten paragraph:

FIG. 9 is a cross-sectional view ~~for simplistically a~~ semiconductor device according to another embodiment of the present invention. Referring to FIG. 9, in accordance with another embodiment of the present invention, device isolation layer 202 may be formed in a predetermined region of a semiconductor substrate which may include both N-type and P-type regions 200a and 200b. An outline of the isolation layer 202 may define a plurality of first active regions 204a in the N-type region 200a, and a plurality of second active regions 204b in the P-type region 200b. The N-type region 200a may comprise an N-well where PMOS transistors may be formed. The P-type region may comprise a P-well or a P-type substrate where NMOS transistors may be formed. A first gate pattern g3 may cross each first active region 204a, and a second gate pattern g4 may cross each second active region 204b. First gate pattern g3 may include a first gate electrode 208a crossing first active region 204a, first gate insulation layer 206a intervened between the first gate electrode 208a and a surface of the first active region 204a. A first sidewall spacer 212a may cover a sidewall of the first gate electrode 208a. Each second gate pattern g4 may include a second gate electrode 208b crossing the second active region 204b, a second gate insulation layer 206b intervened between the second gate electrode 208b and a surface of the second active region 204b. Second sidewall spacer 212b may cover a sidewall of the second gate electrode 208b.

Please replace the paragraph beginning on page 12, line 21, with the following rewritten paragraph:

The first gate patterns g3 as well as the P-type source/drain regions 216a disposed in the first active regions 204a constitute PMOS transistors. While in the second active regions 204b, the second gate patterns g4 as well as the N-type source/drain regions 216b constitute NMOS transistors. The portions of device isolation layer 202 adjacent to one of the P-type source/drain regions 216a of each PMOS transistor may be etched to form first recesses 220a, whereas other portions of device isolation layer 202 adjacent to one of the N-type source/drain regions 216b of each NMOS transistor may be etched to form second recesses 220b. Portions of N-type region 200a under the respective P-type source/drain regions 216a neighboring the first recessed may be exposed by the first recesses 220a, and portions of the P-type region 200b under the N-type source/drain regions 216b may be exposed by the second recesses 220b.